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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,527	MIYAKE ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-13,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-13,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claim 16 is rejected under 35 U.S.C. 102(b) as being anticipated by Faraboschi et al, U.S. Patent Number 5,930,508 (herein referred to as Faraboschi).

2. Referring to claim 16 Faraboschi has taught wherein a parallel processor performing parallel processing of one of more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information (Faraboschi figures 4 and 5 abstract column 3 lines 16-25), said parallel processor comprising:

A plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instruction in parallel (Faraboschi figure 1 abstract column 3 lines 16-20 column 4 lines 46-48);

An instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information (Faraboschi figure 7 column 3 lines 16-25 column 7 lines 32-36; the alignment logic 720 acts as the fetch unit);

An interface having effective bits corresponding to the instruction execution units, the effective bits indicating the corresponding instruction execution unit for each instruction word (Faraboschi column 3 lines 25-32, column 4 line 57-column 5 line 11);

Wherein the instruction words fetched by the instruction fetch unit have no attached dispersal information(Faraboschi – column 3 lines 15-25; the delimiter information is part of the instruction words and therefore is not attached to the instruction words, but is simply a part of the instruction words).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6 and 11-13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraboschi in view of Park et al, U.S. Patent Number 5,881,307 (herein referred to as Park).

4. Referring to claims 1 and 12 Faraboschi has taught a parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising (Faraboschi figures 4 and 5 abstract column 3 lines 16-25):

A plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel (Faraboschi figure 1 abstract column 3 lines 16-20 column 4 lines 46-48);

An instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information (Faraboschi figure 7 column 3 lines 16-25 column 7 lines 32-36; the alignment logic 720 acts as the fetch unit); and

An instruction issue unit recognizing and, in accordance therewith, selectively each of the basic instructions supplied from the instruction fetch unit to one of the corresponding instruction execution units to execute the issued basic instruction (Faraboschi column 3 lines 25-32, column 4 line 57-column 5 line 11).

Wherein the instruction issue unit comprises a conversion unit to generate an interface having instruction information based on the instruction words, the instruction information indicating a type of the corresponding instruction execution units (Faraboschi – column 3 lines 15-25; the delimiter information is part of the instruction words).

5. Faraboschi has not explicitly taught wherein the instruction issue unit further comprises an interface having effective bits, the effective bits indicating availability of the corresponding instruction execution units. Park has explicitly taught wherein the instruction issue unit further comprises an interface having effective bits, the effective bits indicating availability of the corresponding instruction execution units (Park column 5 lines 36-54; the scoreboard as taught by Park would indicate the available resources by some bits, since in digital processing, which all of the reference used pertain to, bits are used to indicate information and data through binary logic). It would have been obvious to one of ordinary skill in the art at the time of the invention looking at Faraboschi to recognize that some interface would be required between the issue unit, or the buffers holding the instructions, to indicate that the functional units were ready for the next instruction. If the functional units required were not available, or were not ready, for the next instruction, then issuing the next instruction would cause errors in the system. Looking at figure 7 of Faraboschi, one can see that there is a buffer leading into the functional unit. It is obvious that some unit or piece of logic could be used to indicate when to send the next

instruction, which is shown by Park. Since Faraboschi lacks the details of when the issuing unit should know exactly when to send the instruction, one of ordinary skill in the art at the time of the invention would have looked to Park for the missing details. Park teaches a resource scoreboard, which indicates if a resource is ready for an instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have an interface for indicating if a functional unit is available to prevent errors that would occur from an issuing unit sending an instruction to a functional unit before it has completed execution on a previous instruction.

6. Referring to claim 2 Faraboschi has taught wherein the plurality of instruction execution units all have the same structure (Faraboschi column 4 lines 46-50; the execution units may include two or more arithmetic units for parallel computation, and it would be inherent that the arithmetic units would perform the same functions, and does not necessarily include the multipliers since it is stated as the arithmetic units and/or multipliers).

7. Referring to claim 3 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the plurality of instruction execution units (Faraboschi figures 6 and 7, column 3 lines 20-25 and column 4 line 57-column 5 line 25 column 5 lines 52-60 and column 7 lines 32-44; figure 6 is represented in figure 7 by block 720, which is the alignment means, or logic, and has the same functionality as the fetch

unit as described by applicant), and then supplies the rearranged basic instructions to the instruction issue unit (Faraboschi column 3 lines 23-32 and column 7 lines 37-44).

8. Referring to claim 4 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction issue unit rearranges the basic instructions contained in each of the instruction words supplied from the instruction fetch unit, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (Faraboschi figure 4 reference number 740 and column 7 lines 37-44; the expansion block 740 acts as the issue unit as described by applicant).

9. Referring to claim 5 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the instruction execution units (Faraboschi figures 6 and 7, column 3 lines 20-25 and column 4 line 57-column 5 line 25 column 5 lines 52-60 and column 7 lines 32-44; figure 6 is represented in figure 7 by block 720, which is the alignment means, or logic, and has the same functionality as the fetch unit as described by applicant), and then supplies the rearranged basic instructions to the instruction issue unit (Faraboschi column 3 lines 23-32 and column 7 lines 37-44); and

The instruction issue unit further rearranges the basic instructions contained in each of the instruction word supplied from the instruction fetch unit, in accordance with the arrangement

of the instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (Faraboschi figure 4 reference number 740 and column 7 lines 37-44; the expansion block 740 acts as the issue unit as described by applicant).

10. Referring to claim 6 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction fetch unit fetches an instruction word that contains basic instruction arranged in advance in accordance with the arrangement of the instruction execution units (Faraboschi column 4 line 57-column 5 line 25; since the different syllables S1, S3, etc. already have the dispersal bit sets that include the functional unit where the syllable is to be executed, they are already aligned, or arranged in accordance with the execution units).

11. Referring to claim 11 the combination of Faraboschi and Park has taught wherein a first instruction word format is converted into a second instruction word format by the table, the first instruction word format indicating an arrangement of the instruction words from the instruction fetch unit, and the second instruction word format indicating an arrangement of instruction words which corresponds to the instruction execution units (Faraboschi Figure 4, column 4 line 57-column 5 line 18).

12. Referring to claim 12 the combination of Faraboschi and Park has taught wherein the instruction issue unit further comprises a conversion unit for converting a first instruction word format into a second instruction word format on the basis of effective bits, corresponding to the instruction execution units, indicating whether the corresponding instruction execution unit is available (Faraboschi Figure 4, column 4 line 57-column 5 line 18).

13. Referring to claim 13 the combination of Faraboschi and Park has taught wherein the first instruction word format indicates an arrangement of instruction words from the instruction fetch unit, and the second instruction word format indicates an arrangement of instruction words which corresponds to the instruction execution units (Faraboschi Figure 4, column 4 line 57-column 5 line 18).

14. Referring to claim 15 Faraboschi has taught wherein the instruction issue unit issues the basic instructions to the corresponding instruction execution unit based on the interface (Faraboschi column 3 lines 25-32, column 4 line 57-column 5 line 11).

15. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraboschi in view of Park in further view of Nair et al, "Exploiting Instruction Level Parallelism in Processors by Caching Scheduled Groups" (herein referred to as Nair).

16. Referring to claim 7 the combination of Faraboschi and Park has not explicitly taught wherein, depending on the type of basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of the basic instruction being currently executed is completed. However, Faraboschi has taught using different execution units to perform different functions (Faraboschi column 4 lines 46-53; arithmetic units and multipliers). Therefore, issuing the basic instruction to an execution unit is dependent on the type of basic instruction that is performed by the execution unit. Also Faraboschi taught a buffer to hold the basic instructions awaiting the execution unit (Faraboschi figure 7 reference number 750), where the buffer holds the basic instructions issued by the processor before the execution is completed with the current instruction. Nair has taught has taught wherein, depending on the type of basic instruction being currently executed by one of

the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of a basic instruction being currently executed is completed (Nair page 18 column 2 line 2-page 19 column 2 line 1; Nair teaches that each functional unit performs only a subset of all operations performed by the processor; Nair also teaches that scheduling instructions basically involves examination of resources needed by each instruction, so that if some resources are available to begin execution on the next instruction if those are the resources required by the next instruction, even if the previous instruction is still executing; this goes along with the teaching of the Applicant on pages 12-13 from which claim 7 is assumed to have originated from). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Nair with the teachings of the combination of Faraboschi and Park to issue instructions based on the type of instruction before a previous instruction is done executing. Issuing instructions before the previous instruction is completed is known as pipelining, or sometimes micro- pipelining, and increases throughput of the execution units since the instructions do not have to wait for the previous instruction to completely finish before starting execution. Also, by having certain execution units perform a subset of all the functions of the processor, the plurality of execution units take up less space, since it does not require all of the functionalities to perform all of the functions of the processor (Nair page 18 column 2 paragraph 1-2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to issue an instruction to a execution unit designated for certain operations, and to issue instructions before the previous instruction is completed to decrease complexity of the execution units to save production costs, and to increase throughput which reduces execution time, respectively.

17. Referring to claim 8 the combination of Faraboschi and Park and Nair has taught wherein, if a supplied basic instruction does not have data dependency or control dependency, or does not share resources with a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues the supplied basic instruction before the execution of the basic instruction being currently executed is completed (Nair page 19 column 2 lines 1-8; Nair teaches that if an instruction is dependent on data currently being executed, that is not issued, but if it is not dependent on the instructions currently being executed, then the instruction is issued).

Response to Arguments

19. Applicant's arguments filed 01/16/04, paper number 10, have been fully considered but they are not persuasive.

20. In the remarks, in regard to the rejection of claim 1, Applicant argues in essence that:

"This is in direct contract with Faraboschi, which apparently has no such 'conversion unit to generate an interface having effective bits and instruction information based on the instruction words,' but instead merely disperses instruction words according to dispersal codes that have already been attached to the instruction words themselves before being fetched by an instruction fetch unit."

21. This is not found persuasive. Faraboschi's dispersal codes are part of the instruction word, as pointed out by Applicant, in column 3 lines 15-25. Therefore, the instruction information, or dispersal codes, would have come from the instruction words. So Faraboschi would overcome the instruction information in claim 1 as claimed.

In addition, the specification on pages 14-16 teaches that the execution units supply the bits that indicate whether the execution units are available. Therefore the claims are interpreted as the effective bits indicating availability coming from the execution units, and the instruction

information coming from the instruction words. The Park reference is then used in combination with Faraboschi to overcome the part of the limitation including the effective bits.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness
Examiner
Art Unit 2183
February 5, 2004

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SUPERVISORY PATENT EXAMINER
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